THAT WHICH IS CLAIMED IS:

1. Method of reading sequentially from a memory (10) implementing an incremental address counter (12), characterized in that an address jump comprises the following steps:

(a) detecting an address jump signal,

(b) incrementing the incremental address counter (12),

(c) reading the content (28) of the memory (10) at the incremented address,

(d) transferring (34, 32) the content read at the incremented address into the incremental address counter (12), and

(e) reading the content (28) of the memory (10) at the address contained in the incremental address counter (12).

2. Method according to claim 1, characterized in that step (a) comprises decoding an instruction code.

3. Method according to claim 1 or 2, characterized in that step (b) comprises incrementing by at least one unit the incremental address counter.

4. Device for reading sequentially from a memory (10) comprising an input register (14) containing an instruction code and a memory (10) address code, an incremental address counter of the memory (10) which receives the address code from the input register (14), an output register (28) of the memory (10) which records signals read at the address indicated by the incremental address counter (12), characterized in that it further comprises:

- a detection circuit (30) for detecting an address jump instruction and supplying an

incrementation signal for incrementing the incremental address counter (12), and

- means (34, 32) for transferring the content read at the incremented address into the incremental address counter (12).

5. Device according to claim 4, characterized in that the address jump instruction detection circuit is a decoder circuit.

6. Device according to claim 4 or 5, characterized in that the means for transferring the content read at the incremented address into the incremental address counter comprises:

- a logic gate (34) for transferring in parallel the content of the output register (28) corresponding to the content at the incremented address, and

- a multiplexer circuit (32) for directing to the incremental address counter (12) either the address code contained in the input register (14) or the address code contained at the incremented address.